CML Microcircuits

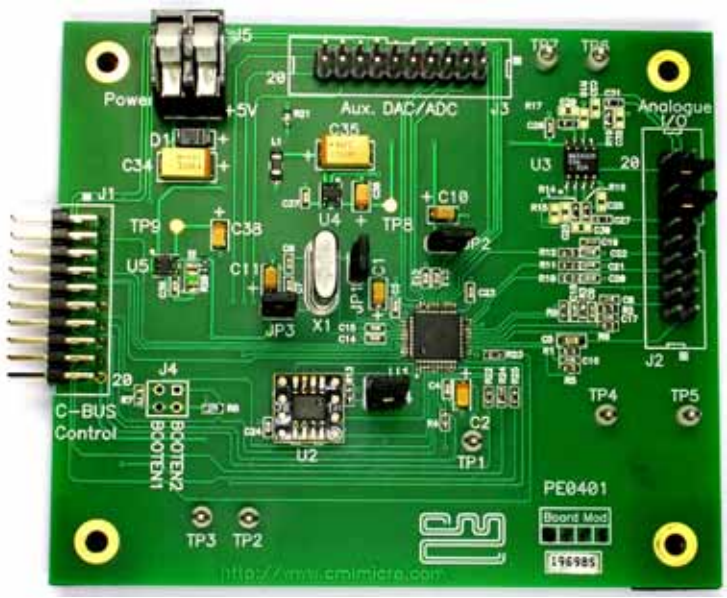
COMMUNICATION SEMICONDUCTORS

PE0401
Platform Evaluation Kit for CMX704x Range

UM0401/4 September 2008 Provisional Issue

Features

- **CMX704x *FirmASIC*® product range evaluation**
- **Serial Flash Option for Function Image™**
- **On-board supply regulators operate from a single 5 volt supply**
- **Command and control by PC via the PE0002 interface card or user's µC development application or emulator**
- **In-circuit Serial Flash Programming**
- **On-board access to all CMX704x signals, commands and data**



1. Brief Description

The PE0401 Platform Evaluation Kit is designed to assist in the evaluation and application development of the CMX704x range of *FirmASIC*® products. The kit is in the form of a populated PCB comprising a CMX704x IC and appropriate supporting components and circuitry.

The board also incorporates all of the necessary power-supply regulation facilities for operation from a single 5 volt supply.

The board is fitted with a C-BUS connector allowing the PE0401 to be operated by connection to either of the two C-BUS ports on a CML PE0002 Interface Card, and used with the associated PC GUI software, or by direct connection between the CMX704x C-BUS and the user's µC development application or emulation system.

The CMX704x Function Image™ (FI) can be loaded, on power-up, directly into the on-board target IC (CMX704x) using the PE0002 interface or the user's system. Alternatively, it can be automatically loaded from the on-board serial Flash memory, on power-up. In this case, the on-board serial Flash memory has to be pre-loaded with the FI by using a suitable third party programmer or by using the 'Program Serial Memory' tab on the PE0002 GUI software. This software is available from the CML website.

Function Images™ suitable for the CMX704x range of products can be downloaded from the CML Project Resource Portal.

CONTENTS

It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

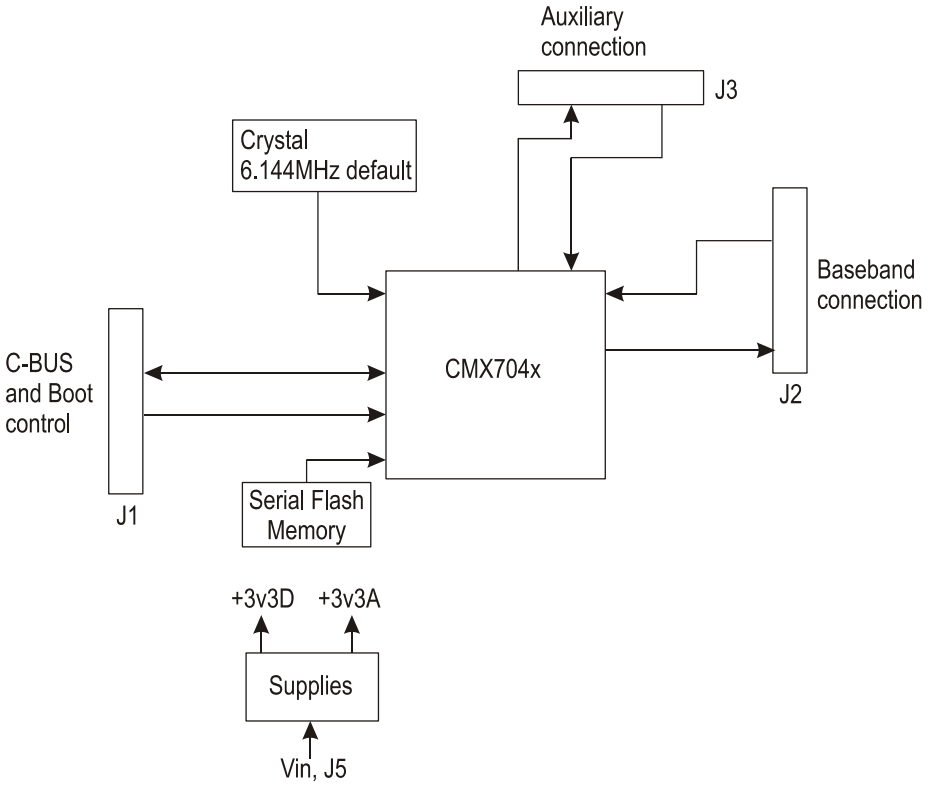


Figure 1 Block Diagram

2. Preliminary Information

The PE0401 is designed to support the CMX704x range of *FirmASIC*® devices using their respective Function Images™.

The CMX704x IC fitted to the PE0401 is a special evaluation IC representing the architecture of all CMX704x series ICs. The functionality of this evaluation IC is obtained from the relevant Function Image™; evaluation FIs are downloaded from the CML Project Resource Portal. Each Function Image™ can represent a different set of features.

2.1 Laboratory Equipment

The following laboratory equipment is needed to use this evaluation kit:

A 5 Volt dc regulated power supply.

If the PE0401 is being used with the PE0002 Interface Card, the following items will also be required:

1. An IBM compatible PC equipped with a USB port and with one of the following Windows operating systems installed - 2000sp4 or XPsp2 and with a minimum screen resolution of 800 x 600 (1024 x 768 recommended).
2. A USB type A male to mini B male cable.
3. Software application **`ES000220.exe`**, or later version, installed on the PC.

For loading a Function Image™ into the PE0401 on-board Flash memory, the 'Program Serial Memory' tab in the above software application should be used.

Also, the "thick stub" application software **`FI_FLASH_10.h`** (or later version), available from the CML website, will first need to be loaded into the CMX704x via the PE0002, in order to be able to program the PE0401 Flash memory with the target Function Image™.

If the PE0401 is not being used with the PE0002 Interface Card, the "thick stub" application software **`FI_FLASH_10.h`** (or later version) will still need to be loaded into the CMX704x, in order to be able to program the PE0401 Flash memory with the target Function Image™. Instructions for loading this software are the same as loading a FI directly into the CMX704x. When this is done, executing this software will load the Function Image™ into the PE0401 on-board Flash memory.

2.2 Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation:

2.2.1 Static Protection

This product uses low power CMOS circuits which can be damaged by electrostatic discharge. Partially damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

2.2.2 Contents - Unpacking

Please ensure that you have received all of the items listed on the separate information sheet (EK0401) and notify CML within 7 working days if the delivery is incomplete.

2.3 Approvals

This product is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements, which may apply to this product.

3. Quick Start

This section is divided into two sub-sections. The first is for those users who are using the PE0401 with a PE0002 controller card and its Windows PC GUI software. The second is for users who are using the PE0401 by itself, without the PE0002.

3.1 With PE0002

Note that the C-BUS connector J1, a right angle header, of the PE0401 is designed to plug directly into socket J5 (C-BUS 1 port) or socket J3 (C-BUS 2 port) of the PE0002.

3.1.1 Setting-Up

- Refer to the PE0002 user manual, and follow the instructions given in the quick start section.

The basic arrangement, when used with the PE0002 is shown below. Note that header J4 is not fitted.

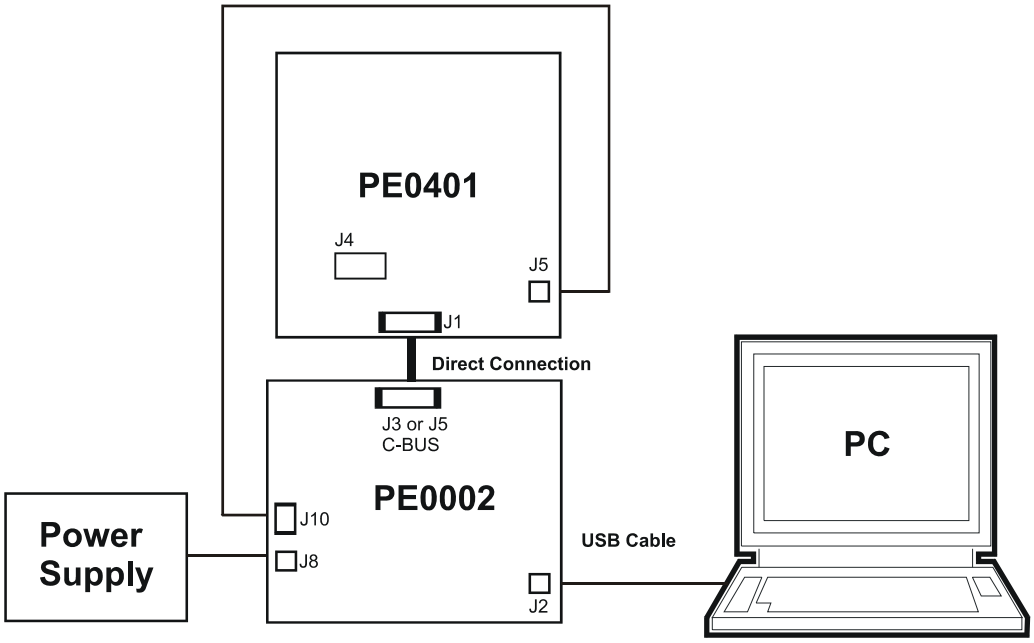


Figure 2 PE0401 used with PE0002

3.1.2 Operation

The Function Image™ (FI) must now be loaded into the CMX704x device. A FI is provided as a 'C' type header file and must be obtained from the CML Project Resource Portal. There are two methods available for loading the FI:

- Directly from a file on the PE0002 host PC to the CMX704x.
- From the on-board PE0401 Flash memory. To use this method the Flash memory must first be programmed with the FI by using the 'Program Serial Memory' tab on the PE0002 GUI software.

The PE0401 should now be ready for evaluation of the CMX704x with the loaded FI.

3.2 Without PE0002

As an alternative to using the PE0002 controller kit, users may control the CMX704x target device with a user-supplied host controller card. C-BUS connections are made via connector J1.

The power-up or boot state of the CMX704x is set via the connector, J1, pins 13 and 14. Consult the relevant CMX704x documentation for valid boot modes. By default, 220kΩ pullup resistors on the PE0401 board provide a '1' state on each of the two BOOTEN pins.

A FI for the CMX704x device must be either included in the customer's host system and loaded into the CMX704x device on power-up or programmed into the on-board Flash memory following the guidelines in the application note: 'Writing a Function Image™ to Serial Memory'.

4. Signal Lists

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J1	1, 15	N/C	-	
	2	CSN	I/P	Chip select. Connects to host μC.
	3	GPIOB	BI	General purpose I/O pin.
	4	CDATA	I/P	Serial Data input. Connects to host μC.
	5	N/C	-	
	6	SCLK	I/P	Serial clock input. Connects to host μC.
	7	N/C	-	
	8	RDATA	O/P	Serial data output. Connects to host μC.
	9	N/C	-	
	10	IRQN	O/P	Interrupt request. Connects to host μC.
	11, 12	GNDD	PWR	Digital supply ground.
	13	BOOTEN1	I/P	CMX704x Hardware Boot Control.
	14	BOOTEN2	I/P	CMX704x Hardware Boot Control.
	16	GPIOA	BI	General purpose I/O pin.
	17	GPIO2	BI	General purpose I/O pin.
	18	GPIO1	BI	General purpose I/O pin.
	19, 20	+3V3D	PWR	3.3V dc digital supply rail.
J2	1	IP1	I/P	Channel 1 inverting input.
	3	IP2	I/P	Channel 2 inverting input.
	5	IP3	I/P	Channel 3 inverting input.
	7	MOD1	O/P	Channel 1 output.
	9	MOD2	O/P	Channel 2 output.
	11	AUDIO	O/P	Channel 3 output.
	13	BUF1IN	I/P	High impedance buffered input.
	15	BUF1OUT	O/P	Buffered output.
	17	BUF2IN	I/P	High impedance buffered input.
	19	BUF2OUT	O/P	Buffered output.
	2, 4, 6, 8, 10, 12, 14, 16, 18, 20	GNDA	PWR	Analogue supply ground.

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J3	1	AUXADC4	I/P	Auxiliary ADC input.
	2	AUXDAC1	O/P	Auxiliary DAC output.
	3	AUXADC3	I/P	Auxiliary ADC input.
	4	AUXDAC2	O/P	Auxiliary DAC output.
	5	AUXADC2	I/P	Auxiliary ADC input.
	6	AUXDAC3	O/P	Auxiliary DAC output.
	7	AUXADC1	I/P	Auxiliary ADC input.
	8	AUXDAC4	O/P	Auxiliary DAC output.
	9, 10	GNDA	PWR	Analogue supply ground.
	11, 12	N/C	-	
	13, 14	GNDD	PWR	Digital supply ground.
	15	GPIOB	BI	General purpose I/O pin.
	16	GPIOA	BI	General purpose I/O pin.
	17	GPIO2	BI	General purpose I/O pin.
	18	GPIO1	BI	General purpose I/O pin.
	19	SYSCLK1	O/P	CMX704x system clock 1 output.
	20	SYSCLK2	O/P	CMX704x system clock 2 output.
J5		+V	PWR	External supply voltage.
		GNDD	PWR	External supply ground.

TEST POINTS		
Test Point Ref.	**Default Measurement**	**Description**
TP1	2.5V	CMX704x internally generated voltage.
TP2	0V	GNDD, digital ground.
TP3	0V	GNDD, digital ground.
TP4	0V	GNDA, analogue ground.
TP5	0V	GNDA, analogue ground.
TP6	0V	GNDA, analogue ground.
TP7	0V	GNDA, analogue ground.
TP8	3.3V	Output from on-board regulator. DC supply voltage for analogue rail.
TP9	3.3V	Output from on-board regulator. DC supply voltage for digital rail.
TP10	0V	GNDA, analogue ground.
TP11	0V	GNDA, analogue ground.
TP12	0V	GNDD, digital ground.
TP13	0V	GNDD, digital ground.

JUMPERS/LINKS			
Jumper Ref.	**Positions**	**Default Position**	**Description**
JP1	1-2	short	Disconnect to supply external clock source to CMX704x.
JP2	1-2	short	Isolates analogue supply rail from CMX704x.
JP3	1-2	short	Isolates digital supply rail from CMX704x.
JP4	1-2	open	Write protects the serial Flash memory (when shorted).
Connector Ref.	**Positions**	**Default Position**	**Description**
J2	13-14	short	Ground input to uncommitted buffer1.
	17-18	short	Ground input to uncommitted buffer2.

LEDs	
LED Ref.	**Description**
D2	Indicates that digital supply voltage is present.

Notes: I/P = Input
O/P = Output
BI = Bidirectional
N/C = Not connected
PWR = Power supply connection

5. Circuit Schematics and Board Layouts

For clarity, circuit schematics are available as a separate high resolution pdf file. This can be found on the CML website.

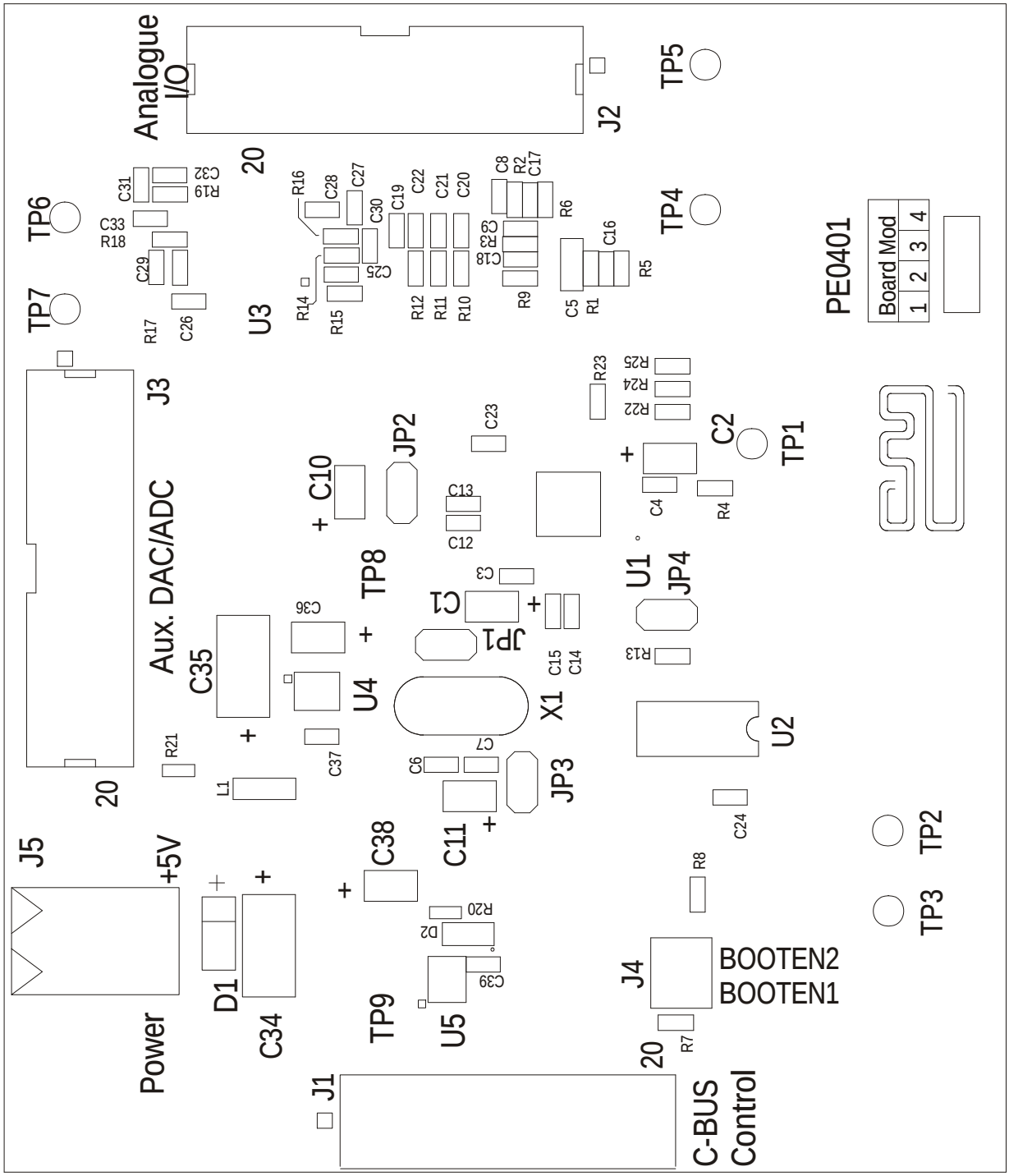


Figure 3 Evaluation Board - Layout

6. Detailed Description

6.1 Hardware Description

6.1.1 Power Supplies

The board is fitted with two voltage regulators. U4 and U5 provide the analogue and digital supply rails respectively. The input to these two regulators is provided by an external 5V dc regulated power supply, which is connected to the board via connector J5, a snap type connector.

The analogue and digital supply voltage levels can be monitored on test points TP8 and TP9 respectively.

LED illumination confirms the on-board presence of the +3.3V dc digital voltage supply.

6.1.2 Clock Options

The board uses the fitted 6.144MHz crystal as the default clock source for the CMX704x. Alternatively, jumper JP1 can be removed and using an appropriate lead, an external clock source with a signal level of less than +3V3D, can be applied between pin 2 of JP1 and GNDD. An alternative clock frequency may be required for the correct operation of some FIs.

6.1.3 Control Interface

The C-BUS and CMX704x boot control signals are brought out on connector J1. This is a right angle male header designed to plug directly into the PE0002 controller card, which has a matching female header. Note that power is not supplied across this connector, so PE0002 and PE0401 will need separate power supply connections.

If the PE0002 is not being used to control the PE0401 then the boot state of the CMX704x device should be set manually by controlling pins 13 and 14 of connector J1. Please refer to the relevant FI documentation for further details of the permissible boot states.

6.1.4 Signal Interfacing

Connector J3 provides access to Auxiliary ADCs 1 to 4, Auxiliary DACs 1 to 4, the general purpose I/O lines and the synthesized digital clock outputs of the CMX704x device.

The CMX704x device input amplifiers for IP1, IP2 and IP3 are configured as ac coupled, unity gain, inverting amplifiers. The inputs to these circuits are fed from connector J2. In some applications, it may be preferable to dc couple these inputs by replacing capacitors C5, C8 or C9 with 0R wire links. If this is done, users should ensure that dc offsets do not reduce the dynamic range of these inputs.

The CMX704x device outputs, MOD1, MOD2 and AUDIO, are fed through an RC network to connector J2.

A dual op amp IC is fitted to the board, with both amplifiers configured as unity-gain buffers. It is possible to set up other op amp based configurations with the addition of passive components to the PCB footprints provided. It is recommended that 0603 sized surface mount components are used. Access to the input and output of each of these uncommitted amplifiers is also provided at connector J2.

6.1.5 Serial (Flash) Memory

The PE0401 is shipped with a blank serial Flash memory, U2. If using the PE0002 to control the PE0401 then the 'Program Serial Memory' tab in the GUI software (**`ES000220.exe`**) can be used

to program the Flash memory in-circuit (described later). The Flash memory can be write protected by fitting a jumper to JP4.

Instead of using serial Flash memory, FIs may be loaded directly into the CMX704x device via J1, the C-BUS interface. However, when power is removed from the PE0401, the FI will be erased from the CMX704x device and will need to be re-loaded when power is re-applied to the PE0401.

6.2 Adjustments and Controls

None

6.3 Function Image™

There are two methods by which a FI may be loaded into the CMX704x device, using the PE0002 PC Interface card:

Load Function Image™ via C-BUS

Use the 'Function Image™ Load' tab. Select Function Image™ Source: “C-BUS”.

- Enter the name of the file containing the Function Image™ , or navigate to the required file name using the ‘Browse’ button.
- Enter the activation code in the lower edit box. Alternatively select one of two previously used codes in the drop down list.
- Select Target Board.
- Click the “Load” button. The progress of the download is shown visually on the progress bar and when the download has completed a message box will be displayed indicating if the result of the download operation was successful or not.

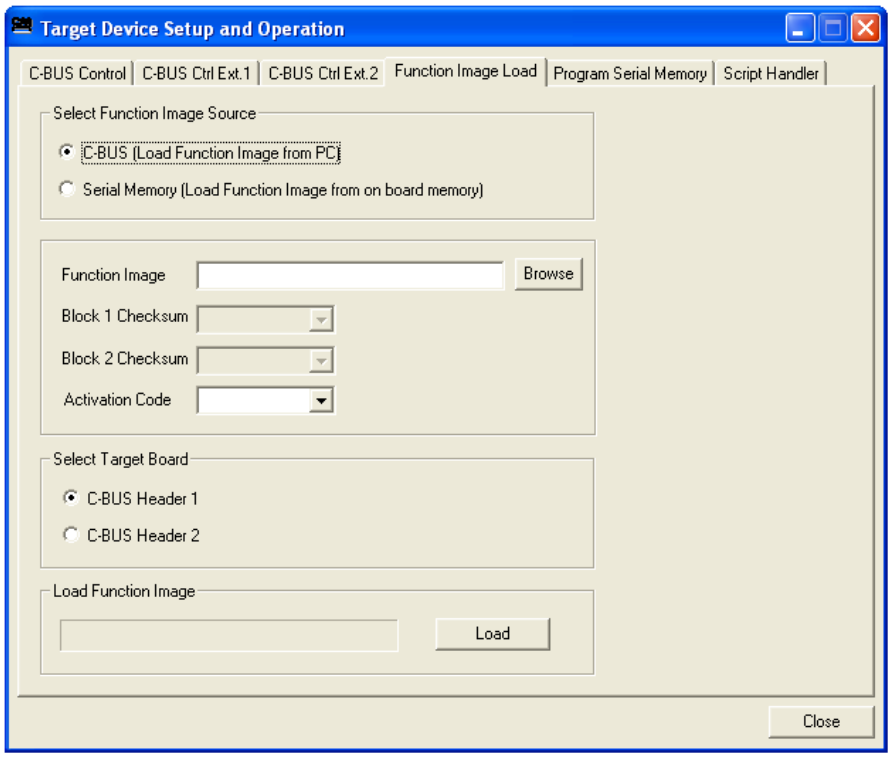


Figure 4 'Function Image™ Load' Tab – via C-BUS

Load Function Image™ from serial memory device

It is assumed that the serial Flash memory has been programmed with the Function Image™ prior to using this load method. This can be carried out with the serial Flash memory in circuit by using the ES0002xx 'Program Serial Memory' tab.

Use the 'Function Image™ Load' tab. Select Function Image™ Source: "Serial Memory".

- Enter the block 1 and block 2 checksum values in the edit boxes. Alternatively select one of two previously used values in the drop down list for each block.
- Enter the activation code in the lower edit box. Alternatively select one of two previously used codes in the drop down list.
- Select Target Board.
- Click the "Load" button. The progress of the download is shown visually on the progress bar and when the download has completed a message box will be displayed indicating if the result of the download operation was successful or not.

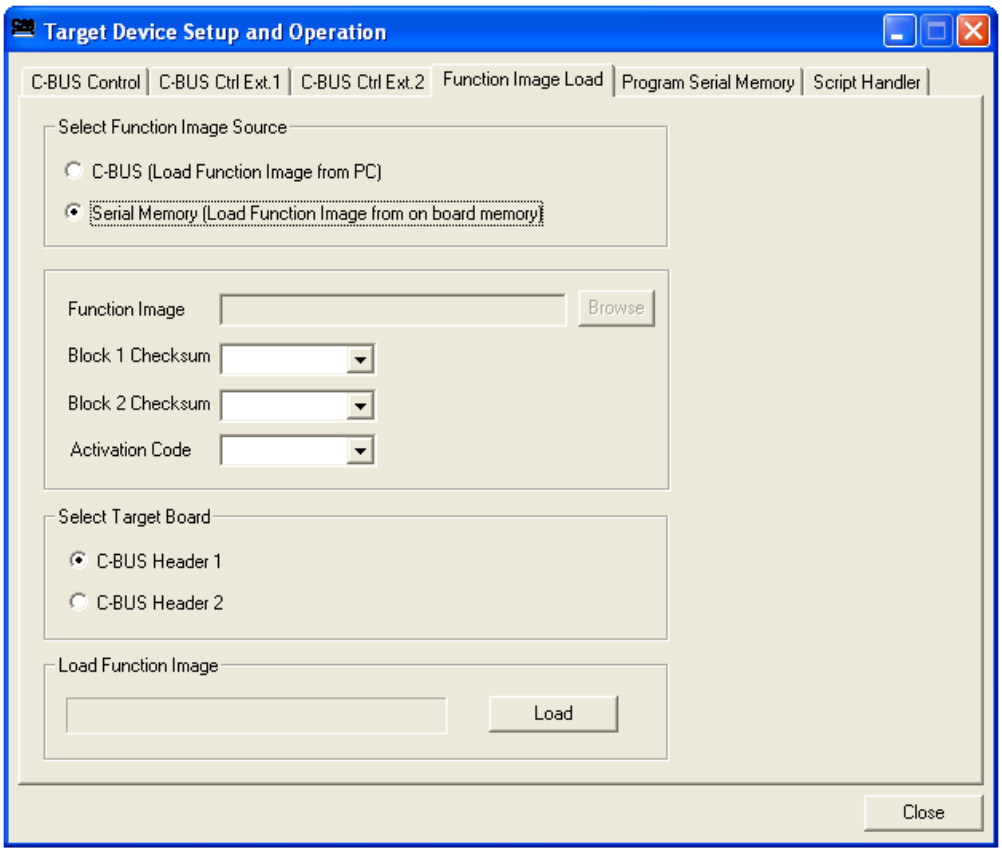


Figure 5 'Function Image™ Load' Tab – from serial memory

Program serial memory

Use the 'Program Serial Memory' tab:

- Enter the name of the file containing the thick stub, or navigate to the required file name using the ‘Browse’ button. This file is in the same ‘C’ language header format as the Function Image™.
- Enter the name of the file containing the Function Image™, or navigate to the required file name using the ‘Browse’ button.
- Enter, in units of MHz, the crystal/clock input frequency of the CMX704x device. The default is 19.2MHz. This will need to be changed to the frequency used on the PE0401 board, which is 6.144MHz, by default. Please note that some FIs may require this frequency to be changed (both on the PE0401 board and in the 'Program Serial Memory' tab).
  The Clk. Divide Setting is dependent on the frequency value which has been entered above and this Clk. Divide Setting will be calculated by the software when the 'Load' button is clicked, requiring no intervention from the user.
- Select Target Board.
- Click the “Load” button.

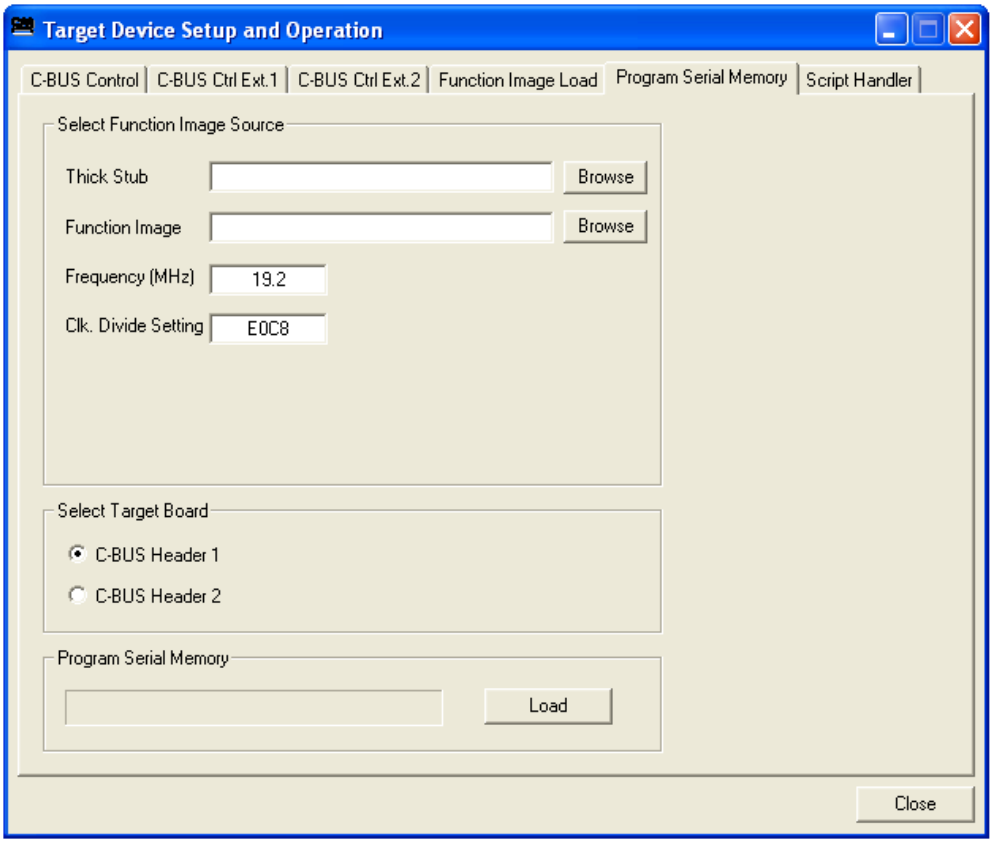


Figure 6 'Program Serial Memory' Tab

Shortly after pressing the Load button, a message box will confirm that the application has loaded the Thick Stub.

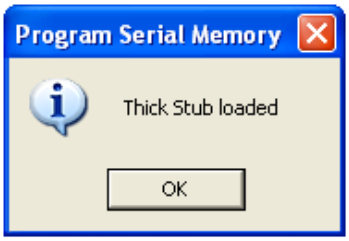


Figure 7 Thick Stub loaded Message Box

Click on the message box OK button and the application will proceed to programme the Function Image™ into the serial memory on the PE0401 card. Progress is shown visually on the progress bar. When programming is complete a message box will be displayed indicating if the operation was successful or not.

Figure 8 Program Serial Memory complete Message Box

6.4 Evaluation Tests

Before a FI is loaded into the CMX704x device, there is a limited functionality which can be demonstrated directly by programming the C-BUS registers. The first group of examples can be used to verify control of the CMX704x via the C-BUS interface. These registers can be programmed by using the 'C-BUS Control' tab in the GUI software.

6.4.1 Write to and Read from a Register

- Write any 16-bit number to register $C0.
  The data transferred to the device on the Command Data pin looks like this:
  { C0 } { <ms byte> } { <ls byte> } ..... Command Data

- The value written to this register (the Powerdown Control register) can be read back from register $C4 by issuing a single command byte, then reading two data bytes from the Reply Data pin, as follows:
  { C4 } ..... Command Data
  { <ms byte> } { <ls byte> } ..... Reply Data

Note that the power consumption of the device will increase once this register has been written to, since some parts of the device will no longer be powersaved.

6.4.2 Check Analogue Path and Set Input Gain

Write 0x4061 to $C0 (Powerdown Control)
Write 0x770F to $B0 (Analogue Gain)
Write 0x0C30 to $B1 (Input Gain and Signal Routing)
Write 0x0008 to $CF (Test Mode)

Apply a 1kHz, audio signal to the input, IP3 (J2 pin 5), at a level of -10dBm (the maximum signal level before distortion is about +1dBm).

Check the audio signal coming out of the AUDIO OUT pin (J2, pin 11). The level should be 5.5dB, below the level of the input signal.

The MOD1 and MOD2 outputs should have no signal on them. All three outputs should have a dc bias level of approximately 1.65 volts.

6.4.3 Check Analogue Path and Set Output Gain

Write 0x03E1 to $C0 (Powerdown Control)
Write 0x410C to $B0 (Analogue Gain)
Write 0x0001 to $CF (Test Mode)

Apply a differential 1kHz, audio signal across the inputs, IP1 (J2, pin 1) and IP2 (J2, pin 2), at a level of 0dBm between them.

The measured differential level between the IP1FB and IP2FB pins can be used as a reference for further measurements. The diagram shown below indicates the positions on the PCB where these measurements can be made.

Check the audio signal coming out of the AUDIO OUT pin (J2, pin 11).
The level should be -9.6dBm.

Check the audio signal coming out of the MOD1 pin (J2, pin 7). The level should be -6.0dBm.

Check the audio signal coming out of the MOD2 pin (J2, pin 9). The level should be -12.0dBm.

The MOD1 and MOD2 outputs should have a DC bias level of approximately 1.65 volts.

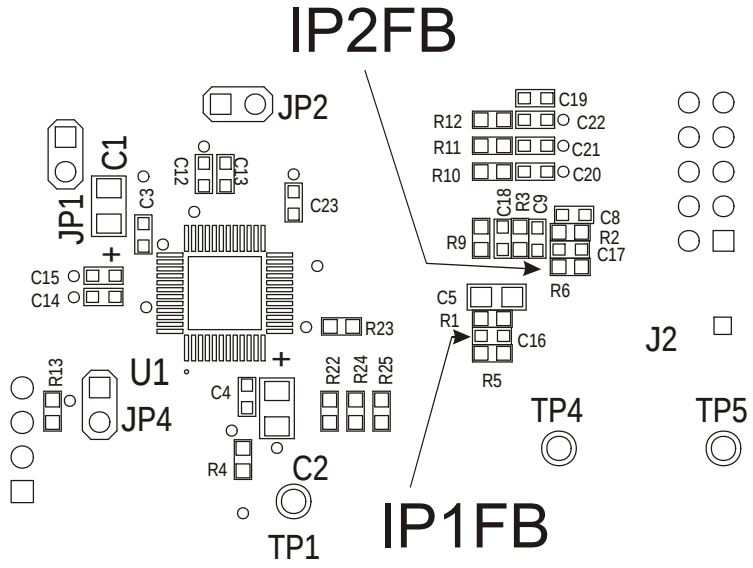


Figure 4 Measurement points for IP1FB and IP2FB signal levels

6.4.4 Generate Two External Digital Clocks

Write 0x0021 to $C0 (Powerdown Control)
Write 0x1900 to $AB (System Clock 1 PLL Configuration)
Write 0xE040 to $AC (System Clock 1 Reference and Source Configuration)
Write 0x0E00 to $AD (System Clock 2 PLL Configuration)
Write 0xE040 to $AE (System Clock 2 Reference and Source Configuration)

With the default 6.144MHz clock input, a digital clock frequency of 4.096MHz should be observed at the AUX/SYS CLOCK 1 output (J3, pin 19) and a frequency of 16.384MHz should be observed at the AUX/SYS CLOCK 2 output (J3, pin 20).

Now write 0xC040 to either $AC or $AE registers, to turn off the CLKOUT1 or CLKOUT2 outputs, respectively.

6.5 Troubleshooting

After loading a Function Image™ the ES0002xx application writes the activation code that has been typed into the Activation Code edit box to the CMX704x device. If this code is incorrect for the Function Image™ that has just been loaded, the CMX704x device will lock up and will not respond to further input from the ES0002xx application. It is recoverable only by closing the ES0002xx application, power cycling the PE0401 and PE0002 cards, and then restarting the application. Keep the power off for at least 10 seconds during this process.

7. Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the Evaluation Kit.

	Min.	Max.	Units
Supply (V_{IN} - V_{SS})	-0.3	9.0	V
Voltage on any connector pin to V_{SS}	-0.3	3.6	V
Current into or out of V_{IN} and V_{SS} pins	0	+0.45	A
Current into or out of any other connector pin	-20	+20	mA

7.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (+V - V_{GND})		4.5	5.5	V
External Clock Frequency		4.0	24.576	MHz

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Evaluation Device Clock Frequency = 6.144MHz, V_{IN} = 5.0V, Tamb = +25°C.

For CMX704x parameters, see relevant CMX704x data sheet.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD}	1	50	55	75	mA
+3V3A		3.15	3.3	3.45	V
+3V3D		3.15	3.3	3.45	V
Analogue Parameters					
Output Impedances					
Mod1, Mod2 and Audio	2	-	100	-	kΩ
Buf1out and Buf2out	4	-	0.1	-	Ω
Input Impedances					
IP1, IP2 and IP3		-	50	-	kΩ
Buf1in and Buf2in	4	1	-	-	MΩ
External Clock Input					
'High' pulse width	3	21	-	-	ns
'Low' pulse width	3	21	-	-	ns
Input impedance		10	-	-	MΩ

Notes:
1. Not including any current drawn from pins by external circuitry.
2. Small signal impedance.
3. Timing for an external input to the CLOCK/XTAL pin.
4. When configured, as supplied, as unity gain buffers.

See relevant CMX704x documentation for C-BUS signal timing information.

About *FirmASIC*®

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

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